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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Response to Request

- On pages 2-3 of the request for consideration, applicant contended that Colmant et al. did not teach or suggest "the queue includes at least one dual-port random access memory (DPRAM) and wherein the number of banks corresponds to a number of address bits allocated in the DPRAM for one or more of the links, and wherein an address in the DPRAM is computed by combining a start address for one of the links and bits corresponding to an extra total address".
- The examiner maintained with clarification, these claimed limitations as were previously disclosed in the prior prosecution whereby Colmant et al. taught the limitations of the claim except DPRAM, address bits and address in the DPRAM which were taught by Sakai in that the queue includes at least one dual-port random access memory (DPRAM) (Fig. 7, DPRAM 51) and wherein the number of banks corresponds to a number of address bits (memory reads data stored from storage means arranged on a bit by bit (bank) basis for each frame, paragraph [0038], page 2, lines 3-6) allocated in the DPRAM for one or more of the links (Fig. 7, 52 m-bit signal (link) data, paragraph [0085], page 5, lines 5-6), and wherein an address (Fig. 7, 53 address counter) in the DPRAM is computed by combining a start address (Fig. 7, 54 address data from the address counter circuit 53, paragraph [0085], page 5, lines 8-10) for one of the links and bits corresponding to an extra total address (Fig. 7, 60

address data from the address counter circuit 59, paragraph [0085], page 5, lines 16-18).

- On page 3-4 of the request for consideration, applicant contended that the cited references did not teach or suggest "selecting a first link, checking whether the link is in use, and if the link is in use, checking whether a second link is in use and increasing a link count until a last link is checked; if the first link is not in use, assigning a desired number of banks to the first link and assigning a start address and an end address to the link; and assigning one or more banks to the second link by increasing a start address and end address of the second link by referring to the end address of the first preceding link".
- The examiner maintained these claimed limitations as were previously disclosed in the prior prosecution.

- On page 4 of the request for consideration, applicant contended that the cited references did not teach or suggest "initializing address-related parameters of each link from a first link to a last link; if the initialization is completed through the last link, starting a read algorithm; checking whether there exists one item of data to be written in the queue beginning with the first link until the last link has been checked; if there exists data to be written, writing the data using a write address and write enable signal and increasing a total address when the writing is completed; setting a write pointer with the increased total address, transmitting the write pointer to a signal

detection unit and checking whether a current address of the link is the highest address of the bank by referring to the total address; and if the current address is the highest address, toggling write carry for the next link, assigning the lowest bits to the total address, or if the current address is not the highest address, checking whether there is data for the next link.

- The examiner maintained with clarification, these claimed limitations as were previously disclosed in the prior prosecution such that initializing address-related parameters (threshold parameter is reset when the base pointer is loaded, column 9, lines 5-6) of each link from a first link to a last link (Fig. 3A, links connected to the queues 1-N); if the initialization is completed through the last link, starting a read algorithm (Fig. 3A, 27 control logic);
- checking whether there exists one item of data to be written in the queue (computation logic comprising a queue manager for handling packet and multimedia data transferred between a host and network system with a base pointer for each queue which is the starting location and a threshold value indicative of data transferred out of the queue, column 3, lines 16-26; efficient queue management algorithm for dynamically allocating and transferring data to the queues with activity, column 3, lines 50-53) beginning with the first link until the last link has been checked; if there exists data to be written, writing the data using a write address (Fig. 5A, QFADDR memory address, column 11, line 12) and write enable signal (queue signal written back to the write parameter RAM, column 11, lines 50-52) and increasing a total address (Fig. 5A, address on signal is increased by fast

incrementing 16, column 11, lines 48-49) when the writing is completed; setting a write pointer with the increased total address, transmitting the write pointer to a signal detection unit (Fig. 3B, computation logic with the write pointer set to the base pointer, increments the memory address to control the base pointer into the write pointer to generate signals to update the queue being serviced, column 3, lines 30-37) and checking whether a current address of the link is the highest address of the bank (Fig. 3B, computation logic 32 increments the memory address, calculates the limit value at the top of the queue which is compared with the incremented memory address and controlling gating the write pointer, column 3, lines 32-36) by referring to the total address; and

- if the current address is the highest address, toggling write carry for the next link, assigning the lowest bits (Fig. 3B, amount filled in the queue is equal to or greater than the threshold, the full sum of the computation logic is zero detected to produce status bits used for handling data to and from the queues, column 3, lines 42-47) to the total address, or if the current address is not the highest address, checking whether there is data for the next link.

- On page 4 of the request for consideration, applicant contended that the cited references did not teach or suggest "address-related parameters include a link start address, a link end address, a total address, and a write carry".
- The examiner maintained these claimed limitations as were previously disclosed in the prior prosecution.

- On page 4 of the request for consideration, applicant contended that the cited references did not teach or suggest “when the current address of the link has not reached the highest address of the bank, if the restart condition arises, said flexible queue assignment method further comprises initializing address-related parameters of each link”.
- The examiner maintained these claimed limitations as were previously disclosed in the prior prosecution.

- On page 5 of the request for consideration, applicant contended that the cited references did not teach or suggest "generating the empty signal comprises determining a range of each link; from the first link to the last link, comparing the write carry and read carry sequentially and calculating a difference between write pointer and read pointer; and checking existence of data based on the difference of the pointers and generating the empty signal accordingly”.
- The examiner maintained these claimed limitations as were previously disclosed in the prior prosecution.

- On page 5 of the request for consideration, applicant contended that the cited references did not teach or suggest “range of each link indicates a number of banks assigned to each link and is determined by using a start address and an end address of each link”.

- The examiner maintained these claimed limitations as were previously disclosed in the prior prosecution.

- On page 5 of the request for consideration, applicant contended that the cited references did not teach or suggest "determining a range of each link; from the first link to the last link, comparing the write carry and read carry sequentially and calculating a difference of pointers according to the comparison; and if the write carry and the read carry are the same, generating the full signal indicating a full or not-full state depending on whether said difference of pointers is within certain user-specified range".
- The examiner maintained these claimed limitations as were previously disclosed in the prior prosecution.

- On page 5 of the request for consideration, applicant contended that the cited references did not teach or suggest "said difference of pointers is calculated by subtracting the read pointer from the write pointer if the write pointer and the read pointer are the same, or if the write pointer and the read pointer are not the same by calculating the difference of the write pointer and the read pointer reflecting the range of link".
- The examiner maintained these claimed limitations as were previously disclosed in the prior prosecution.

- On page 6 of the request for consideration, applicant contended that the cited references did not teach or suggest "checking whether the empty signal is in the not-empty state from the first link to the last link; if a link is detected to be in the not-empty state, reading data through read address and read enable signal connected to the queue; increasing read address and total address by the number of data items that have been read and checking whether the current address of the link is equal to the highest address of the bank; and if the current address of the link is equal to the highest address, toggling read carry and initializing total address with the lowest address of the bank, thereby moving to a next link".
- The examiner maintained these claimed limitations as were previously disclosed in the prior prosecution.

LA/la
February 2, 2009